Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-9 (Canceled).

10. (Previously Presented) An MRAM memory array, comprising:

word lines;

bit lines crossing the word lines;

first diodes, each first diode comprising:

a cathode; and

an anode coupled to a corresponding bit line;

second diodes, each second diode comprising:

an anode; and

a cathode coupled to a corresponding word line; and

magnetic tunnel junction memories including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer and the free layer;

each magnetic tunnel junction memory being connected between a first diode at the corresponding crossing bit line and a second diode at the corresponding crossing word line.

11. (Original) The MRAM memory array as claimed in claim 10, wherein the number of diodes is equal to the total number of word lines and bit lines.

12. (Original) The MRAM memory array as claimed in claim 10, wherein the number of magnetic tunnel junction memories is the product of the number of word lines and the number of bit lines.

13. (Original) The MRAM memory array as claimed in claim 10, wherein the numbers of word lines is three and the numbers of the bit lines is two.

14. (Original) The MRAM memory array as claimed in claim 10, wherein the numbers of word lines is three and the number of bit lines is three.

15-16 (Canceled).

17. (Previously Presented) An MRAM memory array, comprising:

a first word line;

a second word line;

a first bit line crossing the first word line, the second word line;

a second bit line crossing the first word line, the second word line;

a first diode having a first cathode, and a first anode coupled to the first bit line;

a second diode having a second cathode, and a second anode coupled to the second bit line;

a third diode having a third anode, and a third cathode coupled to the first word line;

a first magnetic tunnel junction memory connected between the first cathode and the third anode, the first magnetic tunnel junction memory including:

a first pinned layer;

a first free layer; and

a first non-magnetic layer located between the first pinned layer and the first free layer;

the first magnetic tunnel junction memory being connected between the first diode and the third diode;

a second magnetic tunnel junction memory connected between the second cathode and the third anode, the second magnetic tunnel junction memory including:

a second pinned layer;

a second free layer; and

a second non-magnetic layer located between the second pinned layer and the second free layer;

the second magnetic tunnel junction memory being connected between the second diode and the third diode.

18. (Previously Presented) An MRAM memory array comprising:

a plurality of first and second conductive lines;

a plurality of first and second diodes, wherein each of the first diodes comprising a cathode and an anode that couples to a corresponding second conductive line and each of the second diodes comprising an anode and a cathode that couples to a corresponding first conductive line; and

a plurality of magnetic tunnel junction memories, wherein each of the plurality of magnetic tunnel junction memories is connected between a first diode at the corresponding second conductive line and a second diode at the corresponding first conductive line.

19. (Original) The MRAM memory array of claim 18 wherein each magnetic tunnel junction memories includes a pinned layer, a free layer, and a non-magnetic layer located between the pinned layer and the free layer.

20. (Original) The MRAM memory array of claim 18 wherein a total number of first and second switches is equal to a total number of first and second conductive lines.

21. (Original) The MRAM memory array of claim 18 wherein a total number of the magnetic tunnel junction memories is a product of a total number of first conductive lines and a total number of the second conductive lines.

22. (Original) The MRAM memory array of claim 18 further comprising a plurality of segments, wherein each segment includes at least two of the plurality of magnetic tunnel junction memories.

23. (Original) The MRAM memory array of claim 22 wherein the segments are separated by field effect transistors.

24. (Original) The MRAM memory array of claim 22 wherein the segments are separated by diodes.

25. (Canceled).